Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	818	(amorphous adj carbon) and annealing	US-PGPUB; USPAT	OR	ON	2005/03/10 15:48
L2	89	(amorphous adj carbon) and (laser with annealing)	US-PGPUB; USPAT	OR	ON	2005/03/10 14:26
L3	76	2 and @ad<"20031003"	US-PGPUB; USPAT	OR	ON	2005/03/10 15:49
L4	40	(amorphous adj carbon) and annealing	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/10 14:26
L5	5	4 and (laser with annealing)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/10 14:27
L6	724	1 and @ad<"20031003"	US-PGPUB; USPAT	OR	ON	2005/03/10 15:49
L7	648	6 not 2	US-PGPUB; USPAT	OR	ON	2005/03/10 15:19
L8	122	7 and (carbon with (doped or dopant or doping))	US-PGPUB; USPAT	OR	ON	2005/03/10 15:19
L9	59	8 and laser	US-PGPUB; USPAT	OR	ON	2005/03/10 15:42
L10	4	((laser adj annealing) same (continuous adj wave) same electromagnetic) and @ad<"20031003"	US-PGPUB; USPAT	OR	ON	2005/03/10 15:43
L11	105	((amorphous adj carbon) with (nitrogen or boron or phosphous or fluorine)) and annealing	US-PGPUB; USPAT	OR	ON	2005/03/10 16:09
L12	88	11 and @ad<"20031003"	US-PGPUB; USPAT	OR	ON	2005/03/10 16:09
L13	40	12 and laser	US-PGPUB; USPAT	OR	ON	2005/03/10 15:49
L14	34	13 not 3	US-PGPUB; USPAT	OR	ON	2005/03/10 15:50
L16	34	((amorphous adj carbon) with (nitrogen)) and annealing	US-PGPUB; USPAT	OR	ON	2005/03/10 16:09
L17	30	16 and @ad<"20031003"	US-PGPUB; USPAT	OR	ON	2005/03/10 16:09

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	818	(amorphous adj carbon) and annealing	US-PGPUB; USPAT	OR	ON	2005/03/10 15:48
L2	89	(amorphous adj carbon) and (laser with annealing)	US-PGPUB; USPAT	OR	ON	2005/03/10 14:26
L3	76	2 and @ad<"20031003"	US-PGPUB; USPAT	OR	ON	2005/03/10 15:49
L4	40	(amorphous adj carbon) and annealing	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/10 14:26
L5	5	4 and (laser with annealing)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/10 14:27
L6	724	1 and @ad<"20031003"	US-PGPUB; USPAT	OR	ON	2005/03/10 15:49
L7	648	6 not 2	US-PGPUB; USPAT	OR	ON	2005/03/10 15:19
L8	122	7 and (carbon with (doped or dopant or doping))	US-PGPUB; USPAT	OR	ON	2005/03/10 15:19
L9	59	8 and laser	US-PGPUB; USPAT	OR	ON	2005/03/10 15:42
L10	4	((laser adj annealing) same (continuous adj wave) same electromagnetic) and @ad<"20031003"	US-PGPUB; USPAT	OR	ON	2005/03/10 15:43
L11	105	((amorphous adj carbon) with (nitrogen or boron or phosphous or fluorine)) and annealing	US-PGPUB; USPAT	OR	ON	2005/03/10 16:09
L12	88	11 and @ad<"20031003"	US-PGPUB; USPAT	OR	ON	2005/03/10 16:09
L13	40	12 and laser	US-PGPUB; USPAT	OR	ON	2005/03/10 15:49
L14	34	13 not 3	US-PGPUB; USPAT	OR	ON	2005/03/10 15:50
L16	34	((amorphous adj carbon) with (nitrogen)) and annealing	US-PGPUB; USPAT	OR	ON	2005/03/10 16:09
L17	30	16 and @ad<"20031003"	US-PGPUB; USPAT	OR	ON	2005/03/10 16:29
L18	837	((rapid adj thermal adj annealing) with laser) and @ad<"20031003"	US-PGPUB; USPAT	OR	ON	2005/03/10 16:29
L19	5	(((rapid adj thermal adj annealing) with laser) with carbon) and @ad<"20031003"	US-PGPUB; USPAT	OR	ON	2005/03/10 16:30

L20	10	(((thermal adj annealing) with laser) with carbon) and @ad<"20031003"	US-PGPUB; USPAT	OR	ON	2005/03/10 16:31
L21	5	20 not 19	US-PGPUB; USPAT	OR	ON	2005/03/10 16:31

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	142	(emissivity with electromagnetic)	US-PGPUB; USPAT	OR	ON	2005/03/10 17:47
L2	21	1 and annealing	US-PGPUB; USPAT	OR	ON	2005/03/10 17:48
L3	21	2 and @ad<"20031003"	US-PGPUB; USPAT	OR	ON	2005/03/10 17:47
L4	317	(emissivity same electromagnetic)	US-PGPUB; USPAT	OR	ON	2005/03/10 17:48
L5	32	4 and annealing	US-PGPUB; USPAT	OR	ON	2005/03/10 17:47
L6	32	5 and @ad<"20031003"	US-PGPUB; USPAT	OR	ON	2005/03/10 17:47
L7	11	6 not 3	US-PGPUB; USPAT	OR	ON	2005/03/10 17:47
L8	177	(emissivity same electromagnetic)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/10 17:48
L9	4	8 and annealing	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/03/10 17:49

US-PAT-NO: 6475888

DOCUMENT-IDENTIFIER: US 6475888 B1

TITLE: Method for forming ultra-shallow junctions using **laser annealing**

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Abstract Text - ABTX (1):

A method for forming an ultra-shallow junction using **laser annealing wherein an amorphous carbon** layer is used as an energy absorber layer comprises the steps of preparing a silicon substrate having isolation layers; forming a gate having a stacked structure of a gate insulating layer, a polysilicon layer and a metal layer on the silicon substrate; forming a sacrificial spacer on the sidewalls of the gate; forming source and drain regions on the silicon substrate regions at both sides of the gate including on the sacrificial spacer; removing the sacrificial spacer; doping impurities to form source/drain extension doping layers on the silicon substrate regions at both sides of the gate; depositing sequentially a reaction preventing layer and an **amorphous carbon** layer as a **laser** absorber layer on the resulting structure; forming source/drain extension doping layers on inner sides of the source and drain regions by performing **laser annealing** in an atmosphere of inert gas or under vacuum; and removing the **amorphous carbon** layer.

TITLE - TI (1):

Method for forming ultra-shallow junctions using **laser annealing**

Brief Summary Text - BSTX (3):

The present invention relates generally to a method for fabricating semiconductor devices and, more particularly, to a method for forming ultra-shallow junctions using **laser annealing with an amorphous carbon** layer as an energy absorber layer.

Brief Summary Text - BSTX (10):

FIG. 1 is a graph plotting sheet resistance versus junction depth in each method for forming ultra-shallow junctions, where reference code A indicates sheet resistance according to junction depths in which RTP is performed to activate doped impurities and reference code B indicates those in which **laser annealing** is performed. Reference code C indicates scaling rule requirements of junction depth and sheet resistance.

Brief Summary Text - BSTX (11):
As shown in FIG. 1, when RTP is performed to activate impurities (A), scaling rule requirements of junction depth and sheet resistance are not fulfilled. However, when **laser annealing** is performed (B), they are fulfilled.

Brief Summary Text - BSTX (12):
A fabrication method for making 70 nm MOSFET using **laser annealing,** as proposed by Bin Yu et al., will be described with reference to FIGS. 2A to 2C. (IEDM 1999, "70 nm MOSFET with Ultra-Shallow, Abrupt, and Super-Doped S/D Extension Implemented by Laser Thermal Process").

Brief Summary Text - BSTX (14):
Referring to FIG. 2B, the first spacer 24 is removed and ions are implanted on the resulting structure to form a SDE doping layer. Then, **laser annealing** is performed to selectively melt and solidify the amorphous surfaces of source/drain regions 25a and 25b, thereby forming a SDE doping layer 26, activated in high concentration on silicon substrate 20 at both sides of gate 23.

Brief Summary Text - BSTX (16):
Ken-ichi Goto proposed a method that the activated dopant concentration of a contact formation region can be maintained at greater than 10.sup.21 /cm.sup.3 by using **laser annealing** after implanting the source/drain ions to improve contact resistance. The ultra-low resistance contact formation method by **laser annealing** will be described with reference to FIGS. 3A to 3C. (IEDM 1999, "Ultra-Low Contact Resistance for Deca-nm MOSFETs by **Laser Annealing**").

Brief Summary Text - BSTX (19):
Referring to FIG. 3C, in order to obtain ultra-low resistance contact, source/drain regions 36a and 36b are formed using **laser annealing** and, at the same time, the surface of the source/drain regions 36a and 36b and the upper surface of gate 33 are transformed into an activated doping layer 37 in a high concentration.

Brief Summary Text - BSTX (21):
The above-mentioned method using **laser annealing** is advantageous to fabrication of a transistor having a silicon gate. However, as shown in FIG. 4, it is difficult to apply to fabrication of a transistor having a metal gate 42d on the upper part of a gate 42, since the metal gate 42d is transformed during **laser annealing** due to the fact that the metal gate 42d has high **laser**

absorption rate. In FIG. 4, reference numeral 40 indicates a silicon substrate, reference numeral 41 is a isolation layer, reference numeral 42a is a gate insulating layer, reference numeral 42b is a silicon gate, reference numeral 42c is a diffusion preventing layer, reference numeral 43a is a source region, reference numeral 43b is a drain region and reference numeral 44 is a SDE doping layer.

Brief Summary Text - BSTX (22):
In order to solve the above-described problems, a method has been developed that includes a step prior to **laser annealing,** in that a metal **laser** absorber layer, for example, a refractory metal thin film such as a Ti/TiN layer, is deposited on the surface of the substrate, thereby preventing an excessive rise in temperature of the metal gate. However, problems exist in that the melting point of Ti is 1,667.degree. C., very similar to that of Si, 1,412.degree. C. Therefore, the Ti components remain in the oxide film after the Ti/TiN layer is removed.

Brief Summary Text - BSTX (24):
Therefore, an object of the present invention is to provide a method for forming an ultra-shallow junction capable of preventing transformation of a metal gate using **laser annealing**.

Brief Summary Text - BSTX (25):
Another object of the present invention is to provide a method for forming an ultra-shallow junction using **laser annealing** to be applied to fabrication of a high performance device without transformation of the gate.

Brief Summary Text - BSTX (26):
In order to achieve the above-described objects, an embodiment of the present invention comprises the steps of: preparing a silicon substrate having isolation layers thereon; forming a gate which has a stacked structure of a gate insulating layer, a polysilicon layer and a metal layer on the silicon substrate; forming a sacrificial spacer on sidewalls of the gate; forming source/drain regions on the silicon substrate region at both sides of the gate including over the sacrificial spacer; removing the sacrificial spacer; doping impurities to form a source/drain extension doping layer on the silicon substrate at both sides of the gate; depositing a reaction preventing layer and an **amorphous carbon** layer as a **laser** absorber layer on the resulting structure; forming source/drain extension doping layers on inner sides of the source/drain regions by **laser annealing**; and removing the **amorphous carbon** layer.

Brief Summary Text - BSTX (27):

Another embodiment of the present invention comprises the steps of: preparing a silicon substrate having trench type isolation layers to define an active region; forming a gate having a stacked structure of a gate insulating layer, a polysilicon layer, a diffusion preventing layer, a metal layer and a hard mask layer on an active region of the silicon substrate; forming a thin oxide layer on the surface of the silicon substrate and the side of the polysilicon layer by performing oxidation processes; depositing a thin silicon nitride layer as an etching preventing layer on the resulting structure; forming a sacrificial spacer on the sidewalls of the gate on which the silicon nitride layer is deposited; forming source/drain regions on the silicon substrate region at both sides of gate including the sacrificial spacer; removing the sacrificial spacer, the silicon nitride layer and the oxide layer formed on the surface of the silicon substrate; doping impurities in low energy to form source/drain extension doping layers on the silicon substrate at both sides of the gate; depositing a silicon oxide layer as a reaction preventing layer and an **amorphous carbon** layer as a **laser** absorber layer on the resulting structure; forming source/drain extension doping layers on inner sides of the source and drain regions by performing **laser annealing**; and removing the **amorphous carbon** layer using an O.sub.2 plasma etching process.

Brief Summary Text - BSTX (28):

Still another embodiment of the present invention comprises the steps of: preparing a silicon substrate having isolation layers thereon; forming a gate having a stacked structure of a gate insulating layer, a polysilicon layer and a metal layer on the silicon substrate; forming source/drain extension doping layers on silicon substrates at both sides of the gate; forming a spacer on the sidewalls of the gate; doping impurities on the silicon substrate at both sides of the gate including the spacer to form source/drain regions; depositing a reaction preventing layer and an **amorphous carbon** layer as an energy absorber layer on the resulting structure; forming source and drain regions on the silicon substrate regions at both sides of gate including the spacer by using **laser annealing**; and removing the **amorphous carbon** layer.

Brief Summary Text - BSTX (29):

Still another embodiment of the present invention comprises the steps of: preparing a silicon substrate having trench type isolation layers thereon to define an active region; forming a gate having a stacked structure of a gate insulating layer, a polysilicon layer, a diffusion preventing layer, a metal layer and a hard mask layer; forming source/drain extension doping layers by doping impurities and rapid thermal treatment on the silicon substrate region at both sides of the gate; depositing a thin silicon nitride layer as an etching preventing layer on the resulting structure; forming a spacer on sidewalls of the gate having the silicon nitride layer thereon; doping impurities to form source and drain regions on the silicon substrate at both sides of gate including the spacer; depositing a silicon oxide layer as a reaction preventing layer and an **amorphous carbon** layer as an energy absorber layer on the resulting structure; forming source and drain regions on the silicon substrate at both sides of the gate including the spacer using **laser annealing**; and removing the **amorphous carbon** layer by using an O.sub.2 plasma etching process.

Detailed Description Text - DETX (2):
FIGS. 5A to 5E are cross-sectional views for showing a method for forming an ultra-shallow junction using **laser annealing** according to an embodiment of the present invention.

Detailed Description Text - DETX (7):
Referring to FIG. 5D, a reaction preventing layer 58 made of a silicon oxide layer is deposited on the resulting structure. An **amorphous carbon** layer 59 (Graphite) is deposited to a thickness of 200 to 400 .ANG. as a laser absorber layer on the reaction preventing layer 58. Then, **laser annealing** is performed in an atmosphere of inactive gas and under vacuum, thereby the inactivated doping layer is activated in a high concentration. As a result, SDE doping layer 57a, is formed on inner sides of source and drain regions 56a, and 56b. Arrows D indicates a path by which energy absorbed in the **amorphous carbon** 59 is transferred to the lower structure and to the silicon substrate 50. During **laser annealing, the amorphous carbon** layer 59 absorbs **laser** energy and the absorbed energy is transferred to the lower structure, thereby activating dopants. Therefore, the metal layer 52d, is not transformed at the gate 52.

Detailed Description Text - DETX (8):
Referring to FIG. 5E, the **amorphous carbon** layer used as a laser absorber layer is removed by an O.sub.2, plasma etching process.

Detailed Description Text - DETX (10):
In the method for forming an ultra-shallow junction using **laser annealing according to the present invention, the amorphous carbon** layer is desirable for a **laser** absorber layer because it has a very high melting point, approximately 3,800.degree. C. and in **laser annealing,** has a diffusion length of 0.02 .ANG. in silicon.

Detailed Description Text - DETX (11):
In short, the laser absorber layer should meet several requirements. First, it should have a high laser absorption rate. Second, the melting point and the

sublimation point thereof should be higher than the maximum temperature in **laser annealing,** for example, 1,300.degree. C. Third, it should have no reaction with a reaction preventing layer, that is, the silicon oxide layer during **laser annealing** and it should be prevented from diffusing into the silicon oxide layer. Finally, when it is removed, it should have a high selective ratio to a lower structure and be capable of easy removal.

Detailed Description Text - DETX (12):
As a result, the **amorphous carbon** layer is desirable for a laser absorber layer in that it has a high laser absorption rate and a high melting point, approximately 3,800.degree. C. Moreover, it has minimal reaction with the silicon oxide layer during short duration **laser annealing** of several nanoseconds (ns) and can be easily removed by O.sub.2, plasma etching.

Detailed Description Text - DETX (13):
It is expected that carbon may react with the oxygen in the silicon oxide layer during annealing. However, in **laser annealing,** the temperature of the **amorphous carbon** layer is about 1,200.degree. C. for several ns and then is decreased to a lower temperature below 200.degree. C. for 300 ns, resulting in minimal reaction between the carbon and the oxygen. In order to completely prevent a reaction between carbon and oxygen, the surface of the silicon oxide layer can be nitrified.

Detailed Description Text - DETX (14):
FIGS. 6A to 6E are cross-sectional views for showing a method for forming an ultra-shallow junction using **laser annealing** according to another embodiment of the present invention.

Detailed Description Text - DETX (18):
Referring to FIG. 6D, a reaction preventing layer 68 made of a silicon oxide layer is deposited on the resulting structure and an **amorphous carbon** layer 69 is deposited as a laser absorber layer on the reaction preventing layer 68. Then, source/drain regions 67a, and 67b, activated in a high concentration are formed on silicon substrate 60 at both sides of gate 62 including the spacer 66 by performing **laser annealing** in an atmosphere of inactive gas and under vacuum.

Detailed Description Text - DETX (19):
Referring to FIG. 6E, the **amorphous carbon** layer used as a laser absorber layer is removed by O.sub.2, plasma etching.

Detailed Description Text - DETX (21):

According to this embodiment, an **amorphous carbon** layer is used as a **laser** absorber layer, thereby preventing transformation of the metal layer of the gate during **laser annealing**. Additionally, the problem of remaining metal ions has been solved, and as a result, it is possible to fabricate a high performance device.

Detailed Description Text - DETX (22):
As described above, according to the present invention, during **laser annealing,** transformation of the metal gate is prevented since an **amorphous carbon** layer is used as a **laser** absorber layer.

Detailed Description Text - DETX (23):
Use of the present inventive method embodiments can solve the problems of remaining metal ions in removing the laser absorber layer since an **amorphous carbon** layer is used as a laser absorber layer.

Claims Text - CLTX (1):
1. A method for forming an ultra-shallow junction using **laser annealing** comprising the steps of: preparing a silicon substrate having isolation layers; forming a gate having a stacked structure of a gate insulating layer, a polysilicon layer and a metal layer on the silicon substrate; forming a sacrificial spacer on the sidewalls of the gate; forming source and drain regions on the silicon substrate regions at both sides of the gate, including on the sacrificial spacer; removing the sacrificial spacer; doping impurities to form a source/drain extension doping layer on the silicon substrate regions at both sides of the gate; depositing sequentially a reaction preventing layer and an **amorphous carbon** layer as a **laser** absorber layer on the resulting structure forming source/drain extension doping layers on inner sides of the source and drain regions by performing **laser annealing** in an atmosphere of essentially inert gas or under vacuum; and removing the **amorphous carbon** layer.

Claims Text - CLTX (2):
2. The method for forming an ultra-shallow junction using **laser annealing** according to claim 1, wherein after the formation of the gate and before the formation of the sacrificial spacer, a thin oxide film is formed on the side of the polysilicon layer by performing selective oxidation processes and a silicon nitride layer is deposited as an etching preventing layer on the resulting structure.

Claims Text - CLTX (3):
3. The method for forming an ultra-shallow junction using **laser annealing**

according to claim 1, wherein the step for formation of the source and drain regions comprises doping of N type or P type dopants on the silicon substrate at both sides of the g at e and performing a rapid thermal treatment.

Claims Text - CLTX (4):
4. The method f or forming an ultra-shallow junction using **laser annealing** according to claim 1, wherein the sacrificial spacer is removed by performing an etching process using HF solution.

Claims Text - CLTX (5):
5. The method for forming an ultra-shallow junction using **laser annealing** according to claim 2, wherein after the sacrificial spacer is removed and before impurities are doped to form the source/drain extension doping layers, the silicon nitride layer formed on the silicon substrate is removed.

Claims Text - CLTX (6):
6. The method for forming an ultra-shallow junction using **laser annealing** according to claim 5, wherein the silicon nitride layer is removed using an anisotropy etching process.

Claims Text - CLTX (7):
7. The method for forming an ultra-shallow junction using **laser annealing** according to claim 1, wherein the step for doping impurities to form the source/drain extension doping layers comprises ion-implantation of N type or P type dopants in low energy or plasma doping.

Claims Text - CLTX (8):
8. The method for forming an ultra-shallow junction using **laser annealing** according to claim 1, herein the reaction preventing layer is a silicon oxide layer.

Claims Text - CLTX (9):
9. The method for forming an ultra-shallow junction using **laser annealing** according to claim 1, wherein the **amorphous carbon** layer is deposited to a thickness of 200 to 400.ANG..

Claims Text - CLTX (10):
10. The method for forming an ultra-shallow junction using **laser annealing** according to claim 1, wherein the **amorphous carbon** layer is removed by etching process using O.sub.2, plasma.

Claims Text - CLTX (11):

11. The method for forming an ultra-shallow junction using **laser annealing** comprising the steps of: preparing a silicon substrate having trench type isolation layers to define an active region; forming a gate having a stacked structure of a gate insulating layer, a polysilicon layer, a diffusion preventing layer, a metal layer and a hard mask layer on the active region of silicon substrate; forming a thin oxide layer on the surface of the silicon substrate and on side of polysilicon layer by performing selective oxidation processes; depositing a thin silicon nitride layer as an etching preventing layer on the resulting structure; forming a sacrificial spacer on sidewall of gate having the silicon nitride layer thereon; forming source/drain regions on the silicon substrate at both sides of gate including the sacrificial spacer; removing the sacrificial spacer, the silicon nitride layer and the oxide layer formed on the surface of the silicon substrate; doping impurities in low energy to form source/drain extension doping layers on the silicon substrate at both sides of the gate; depositing a silicon oxide layer as a reaction preventing layer and an **amorphous carbon** layer as a laser absorber layer on the resulting structure; forming source/drain extension doping layers on inner sides of the source and drain regions by performing **laser annealing** in an atmosphere of inert gas or under vacuum; and removing the **amorphous carbon** layer using an O.sub.2, plasma etching process.

Claims Text - CLTX (12):
12. The method for forming an ultra-shallow junction using **laser annealing** according to claim 11, wherein the sacrificial spacer is removed by an etching process using HF solution and the silicon nitride layer is removed by an anisotropy etching process.

Claims Text - CLTX (13):
13. The method for forming an ultra-shallow junction using **laser annealing** according to claim 11, wherein the step for doping impurities to form the source/drain extension doping layers comprises ion implantation of N type or P type dopants in low energy or plasma doping.

Claims Text - CLTX (14):
14. The method for forming an ultra-shallow junction using **laser annealing** according to claim 11, wherein the **amorphous carbon** layer is deposited to a thickness of 200 to 400.ANG..

Claims Text - CLTX (15):
15. A method for forming an ultra-shallow junction using **laser annealing** comprising the steps of: preparing a silicon substrate having isolation layers thereon; forming a gate having a stacked structure of a gate insulating layer,

a polysilicon layer and a metal layer on the silicon substrate; forming source/drain extension doping layers on the silicon substrate regions at both sides of the gate; forming a spacer on sidewalls of the gate; doping impurities on the silicon substrate at both sides of the gate including the spacer to form source and drain regions; depositing a reaction preventing layer and an **amorphous carbon** layer as an energy absorber layer on the resulting structure; forming source and drain regions on the silicon substrate at both sides of gate including the spacer by performing a **laser annealing** in an atmosphere of inert gas or under vacuum; and removing the **amorphous carbon** layer.

Claims Text - CLTX (16):

16. The method for forming an ultra-shallow junction using **laser annealing** according to claim 15, wherein after the formation of the gate and before the formation of the source/drain extension doping layers, thin oxide layers are formed on the surface of the silicon substrate and on sidewall of the polysilicon layer by performing selective oxidation processes.

Claims Text - CLTX (17):

17. The method for forming an ultra-shallow junction using **laser annealing** according to claim 15, wherein after formation of the source/drain extension doping layers and before formation of the spacer, a silicon nitride layer is deposited as an etching preventing layer on the resulting structure.

Claims Text - CLTX (18):

18. The method for forming an ultra-shallow junction using **laser annealing** according to claim 17, wherein in the formation of the spacer, the silicon nitride layer formed on the surface of the silicon substrate is removed.

Claims Text - CLTX (19):

19. The method for forming an ultra-shallow junction using **laser annealing** according to claim 15, wherein the formation of the source/drain extension doping layers comprises ion implantation of N type or P type dopants in low energy or plasma doping on the silicon substrate at both sides of the gate and performing a rapid thermal treatment.

Claims Text - CLTX (20):

20. The method for forming an ultra-shallow junction using **laser annealing** according to claim 15, wherein the reaction preventing layer is a silicon oxide layer.

Claims Text - CLTX (21):

21. The method for forming an ultra-shallow junction using **laser annealing** according to claim 15, wherein the **amorphous carbon** layer is deposited to a thickness of 200 to 400.ANG..

Claims Text - CLTX (22):
22. The method for forming an ultra-shallow junction using **laser annealing** according to claim 15, wherein the **amorphous carbon** layer is removed by an etching process using O.sub.2, plasma.

Claims Text - CLTX (23):
23. A method for forming an ultra-shallow junction using **laser annealing** comprising the steps of: preparing a silicon substrate having trench type isolation layers to define an active region; forming a gate having a stacked structure of a gate insulating layer, a polysilicon layer, a diffusion preventing layer, a metal layer and a hard mask layer on the active region of the silicon substrate; forming source/drain extension doping layer by doping impurities on silicon substrate at both sides of the gate and by performing a rapid thermal treatment; depositing a thin silicon nitride layer as an etching preventing layer on the resulting structure; forming a spacer on sidewall of the gate and on the silicon nitride layer deposited thereon; doping impurities to form source and drain regions on the silicon substrate at both sides of the gate including the spacer; depositing a silicon oxide layer as a reaction preventing layer and an **amorphous carbon** layer as an energy absorber layer on the resulting structure; forming source and drain regions on the silicon substrate at both sides of the gate including the spacer by performing **laser annealing** in an atmosphere of inert gas or under vacuum; and removing the **amorphous carbon** layer using O.sub.2, plasma etching.

Claims Text - CLTX (24):
24. The method for forming an ultra-shallow junction using **laser annealing** according to claim 23, wherein after the formation of the gate and before the formation of the source/drain extension doping layers, thin oxide layers are formed on the surface of the silicon substrate and on the sidewalls of the polysilicon layer by selective oxidation processes.

Claims Text - CLTX (25):
25. The method for forming an ultra-shallow junction using **laser annealing** according to claim 24, wherein in the formation of the spacer, the silicon nitride formed on the surface of the silicon substrate is removed.

Claims Text - CLTX (26):
26. The method for forming an ultra-shallow junction using **laser annealing**

according to claim 24, wherein the **amorphous carbon** layer is deposited to a thickness of 200 to 400.ANG..

US-PAT-NO: 5569501

DOCUMENT-IDENTIFIER: US 5569501 A
See image for Certificate of Correction

TITLE: Diamond-like carbon films from a hydrocarbon helium plasma

---------- KWIC ---------

Brief Summary Text - BSTX (4):
2. Prior Art Hydrogenated **amorphous carbon** (a--C:H) films, also called diamond-like carbon (DLC) films because of their hardness, have drawn a lot of attention because of their potential use in coatings and semiconductor devices. For these films to be useful in chip process technology or in hostile thermal and mechanical environments, increased thermal stability at high temperatures is necessary.

Drawing Description Text - DRTX (4):
FIG. 3 shows the Forward Recoil Detection (FRD) spectra of a He-- and Ar--PECVD carbon film before **annealing**.

Drawing Description Text - DRTX (5):
FIG. 4 shows the FRD spectra of a He-- and Ar--PECVD carbon film after **annealing**.

Drawing Description Text - DRTX (6):
FIGS. 5 (a) and (b) demonstrate the I-V characteristics of an **amorphous carbon** film/Si heterojunction, wherein FIG. 5(a) represents an n.sup.- and p.sup.- type Si heterojunction and FIG. 5(b) represents an n.sup.+ and p.sup.+ Si heterojunction.

Drawing Description Text - DRTX (7):
FIGS. 6(a) and (b) demonstrate the I-V characteristics of a thin 32 nm **amorphous carbon**/Si (p.sup.-) heterojunction wherein the reverse bias characteristics are shown (a) before and (b) after breakdown.

Detailed Description Text - DETX (21):
In accordance with the present invention, the diamond-like carbon films deposited on the substrate are from about 100 to about 10,000 .ANG. thick.

More preferably, the thickness of the diamond-like carbon coating is from about 400 to about 2000 .ANG.. It should be noted that by changing the resultant film thickness the optical density of the film can be changed. Thus, it is quite possible to tailor make a substrate with a defined optical density by merely increasing or decreasing the thickness of the film. The preferred optical densities of the diamond-like carbon films prepared by the present process are in the range from about 1 to about 3 at a wavelength of 248 nm which corresponds to a film thickness of about 1000 to about 3000 .ANG.. After depositing the diamond-like carbon film onto the substrate, the coated material depending on its application may or may not be annealed. **Annealing** typically involves heating the substrate in an atmosphere of Ar/H.sub.2 at 590.degree. C. for a time period of about 3 to about 5 hours.

Detailed Description Text - DETX (29):

Furthermore, the diamond-like carbon films formed by the present invention may be used as an ideal absorber for deep UV photomasks. Such photomasks will be used as an alternative to chrome mask blanks which are commonly employed in the art. This process will eliminate all of the environmentally hazardous aspects of the chrome deposition, wet and RIE processes. Furthermore, the carbon masks containing the film of the present invention brings with it the high thermal conductivity of diamond as well as the hardness. Thus, these films can also be used as a direct patterned mask material and be ablated using a 193 nm **laser** in a reticle generation machine. The carbon photomask absorber having the film formed from an acetylene/helium plasma are etched at the same rate as photoresist in an oxygen plasma RIE thus eliminating the chrome wet etch and RIE process which produce toxic waste products thus, patterning the mask is a simpler and environmentally more acceptable process.

Detailed Description Text - DETX (40):

FIG. 3 shows the FRD spectra of He-- and Ar--PECVD carbon films. The H content is 26 and 22 at. %, respectively. These numbers are measured by comparison to a known calibrated reference. FIG. 4 shows the same spectra after **annealing** at about 590.degree. C. for 3 hrs in Ar/H.sub.2 ambient. The H content decreased to 17 and 15 at. %, respectively. The Ar-PECVD film became hazy and soft. A roughening of the film may explain the peak asymmetry i.e. the tail, in the spectra of the annealed sample. The He--PECVD sample also lost H but the film was still hard (i.e., it could not be scratched by a razor blade). since both the Ar-- and He--PECVD films lost approximately the same amount of H, the stability can not be attributed only to the H content. H is likely to be in an unbound form for the Ar--PECVD film. **Annealing** at 590.degree. C. of the Ar--PECVD films showed only sp.sup.2 coordination by infrared spectroscopy. The better thermal stability of films prepared in

C.sub.2 H.sub.2 /He mixture indicates that the He may play a major role in stabilizing the sp.sup.3 coordination. Thus, as mentioned previously herein, thermal stability appears to be due to the properties of plasma excited He.

Detailed Description Text - DETX (42):
In summary, it has been shown that the thermal stability of a PECVD **amorphous carbon** film can be greatly enhanced by diluting hydrocarbon gases in He rather than Ar. An **amorphous carbon** film deposited by PECVD of C.sub.2 H.sub.2 /He preserved its hardness after **annealing** at 590.degree. C. This stability appears to be related to a better film nucleation which helps to stabilize the sp.sup.3 tetrahedral coordination, rather than to the H content.

Detailed Description Text - DETX (44):
The following example illustrates the electrical properties on the diamond-like carbon films formed by PECVD from an acetylene/helium gas mixture. The two materials employed in this example comprise an Al/**amorphous carbon**/Cr and Al/**amorphous carbon**/Si. The amorphous diamond-like carbon film was deposited onto the Cr and Si substrate in accordance with the procedure of Example I. The electrical properties of the coated substrates were determined by electron-beam evaporation of Al dots having an area=5.5.times.10.sup.-4 cm.sup.-2 through a metal mask. A capacitance-voltage (C-V) measurement at 1 MHz of the Al/**amorphous carbon**/Cr structure gave a dielectric constant .epsilon.=6.0.+-.0.1 for the **amorphous carbon**. This value compares well with .epsilon.=5.7 reported for diamond (see: S. M., Sze, Physics of Semiconductor Devices, 2nd Cd. (Wiley, N.Y., 1981), Appendix G, p. 849).

Detailed Description Text - DETX (45):
The I-V characteristics of the coated Al/Si structure for four different Si doping concentrations are shown in FIGS. 5(a) and (b) wherein FIG. 5(a) represents an n.sup.- and p.sup.- type Si heterojunction and FIG. 5(b) represents an n.sup.+ and p.sup.+ type Si heterojunction. The silicon doping was .apprxeq.10.sup.15 cm.sup.-3 for n.sup.- and p.sup.- and 10.sup.19 cm.sup.-2 for n.sup.+ and p.sup.+. Note that the I-V characteristics have a strong dependence on the Si substrate **doping** and therefore they can be attributed to the **amorphous carbon**/Si heterojunction and not to the metal/**carbon** interface. FIG. 5b shows the I-V curves at high Si doping. In this case the Fermi level moves closer to the band edges and conditions at the heterojunction are enhanced by tunnelling. This lowers the specific contact resistance of the **amorphous carbon**/Si interface. Thus, a rough estimate of the film resistivity can be obtained by measuring the series resistance associated with the **amorphous carbon**/Si(n.sup.+) heterostructure. This gives .rho..congruent.10.sup.5 .OMEGA..cm which appears to be close to the intrinsic

resistivity of Si .rho.=2.3.times.10.sup.5 .OMEGA..cm.

Detailed Description Text - DETX (46):
FIG. 5a shows that the barrier heights for the amorphous diamond-like carbon film to n- and p- type Si are different. The p- type material gives a barrier height 0.2 eV higher than n- type. This difference can be measured by comparing the reverse bias saturation currents for the n and p materials assuming that the current density is, J, J.varies.exp(-.phi..sub.b /kT).times.[exp(qV/kT)-1] where .phi..sub.b is the barrier at the junction, k is the Boltzmann constant, T is the temperature, q is the charge and V is the applied voltage. Since the doping levels in the n- and p-type Si samples are about the same, the band-edge Fermi level energy differences are also about the same. Also, the optical bandgap from absorption measurements is 1.1 eV for the **amorphous carbon** film which roughly matches the Si bandgap of 1.12 eV (at room temperature). Therefore the 0.2 eV difference can be attributed to an offset between the **amorphous carbon** film and the Si energy band edge; specifically, the electron affinity of the **amorphous carbon** film is less than that of Si by a few tenths of an eV. This would explain the higher barrier observed for the p-type heterostructure when compared to the n-type.

Detailed Description Text - DETX (47):
FIGS. 6(a) and (b) show the I-V characteristic for a heterojunction with a very thin 32 nm amorphous diamond-like carbon film. The silicon is p- type. Under reverse bias, breakdown occurs at 60 V or 19 MV/cm. After breakdown the reverse leakage current increases by approximately two orders of magnitude. The same effect was observed for heterojunctions with a 100 nm film thickness. This implies that breakdown occurs at the junction rather than in the carbon film since no film thickness dependence was observed. Thus, only a very high junction breakdown was obtained under reverse bias. This indicates that the **amorphous carbon** film breakdown is also very close to the diamond breakdown of approximately 10 MV/cm.

Other Reference Publication - OREF (8):
Grill, "Inhomogeneous Carbon Bonding in Hydrogenated **Amorphous Carbon** Films", J. Appl. Phys., 61, pp. 2874-2877 (1987).

DOCUMENT-IDENTIFIER: US 20020037414 A1

TITLE: Low emissivity panel assembly

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Summary of Invention Paragraph - BSTX (20):

[0019] One of the typical requirements for mainstream double-glazed solar efficient units is a low emissivity film, that is, the fourth layer as discussed above. The **emissivity** is the amount of radiation emitted from a substance at a given temperature relative to a black body which radiates all **electromagnetic** energy at any wavelength. The emissivity is one minus the reflectivity. Emissivities vary widely with different metals and over various wavelengths. FIG. 1, for example, shows emissivity values versus wavelength for polished samples of the metals Ag, Al, Cr, Cu, Ti and Zn. The data points have considerable scatter and should be assumed to be only approximate since the numbers are to some extent a function of surface finish, morphology and measurement method. For example, if the metal surface is rough, the emissivity rises.